

CLAIMS:

1. A process of selecting different dual mode test access port domain arrangements within an integrated circuit comprising the steps of;

performing an 1149.1 instruction shift operation through a first dual mode test access port domain arrangement,

performing an 1149.1 instruction update operation at the end of said 1149.1 instruction shift operation, and;

in response to said 1149.1 instruction update operation, selecting a second dual mode test access port domain arrangement which differs from the first dual mode test access port domain arrangement.

2. A process of selecting and communicating to dual mode test access ports within an integrated circuit using first and second protocols comprising the steps of;

communicating to a plurality of dual mode test access ports using said first protocol to select one or more of said plurality of dual mode test access port for communication using said second protocol, and thereafter

communicating to said selected one or more dual mode test access ports using said second protocol.

3. A process of communicating to mixtures or single and dual mode test access ports within an integrated circuit using first and second protocols comprising the steps of;

communicating to a plurality of single and dual mode test access ports using said first protocol to select one or more of said dual mode test access ports for communication using said second protocol, and thereafter

communicating to said selected one or more dual mode test access ports using said second protocol.

4. An integrated circuit comprising;

a first group of one or more dual mode test access ports; and,

a second group of one or more single mode test access ports.

5. An integrated circuit comprising;
a first group of one or more dual mode test access ports;
a second group of one or more single mode test access ports; and,
circuitry operable in a first mode for assessing said first and second groups in combination and in a second mode for accessing said first and second groups individually.

6. An 1149.1 TAP linking module within an integrated circuit comprising;
a serial input terminal and a serial output terminal,
a TAP controller,
an instruction register having a parallel output bus, a serial input connected to said serial input terminal, a serial output, and control inputs connected to said TAP controller,
a multiplexer having a first input connected to said serial input terminal, a second input connected to said instruction register serial output, control input connected to said TAP controller, and an output connected to said serial output terminal, and
a TAP lock circuit having an input connected to the parallel output bus of the instruction register and an output connected to the TAP controller.